AU9412EEP
USB Keyboard/Hub Controller
Technical Reference Manual

Revision 1.03

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1.0 Introduction

1.1. Description

The AU9412EEP is an integrated USB keyboard and 2 port hub controller chip. The AU9412EEP has a built-in default keyboard matrix, so that it can be directly connected to an 18 x 8 keyboard matrix. The keyboard matrix can be customized via an optional external 512-byte serial EEPROM. Downstream ports can be used to connect various USB peripheral devices, such as USB printers, modems, scanners, cameras, mice, and joysticks, to the system without adding external glue logic.

Single chip integration makes the AU9412EEP the most cost effective keyboard/hub solution available in the market.

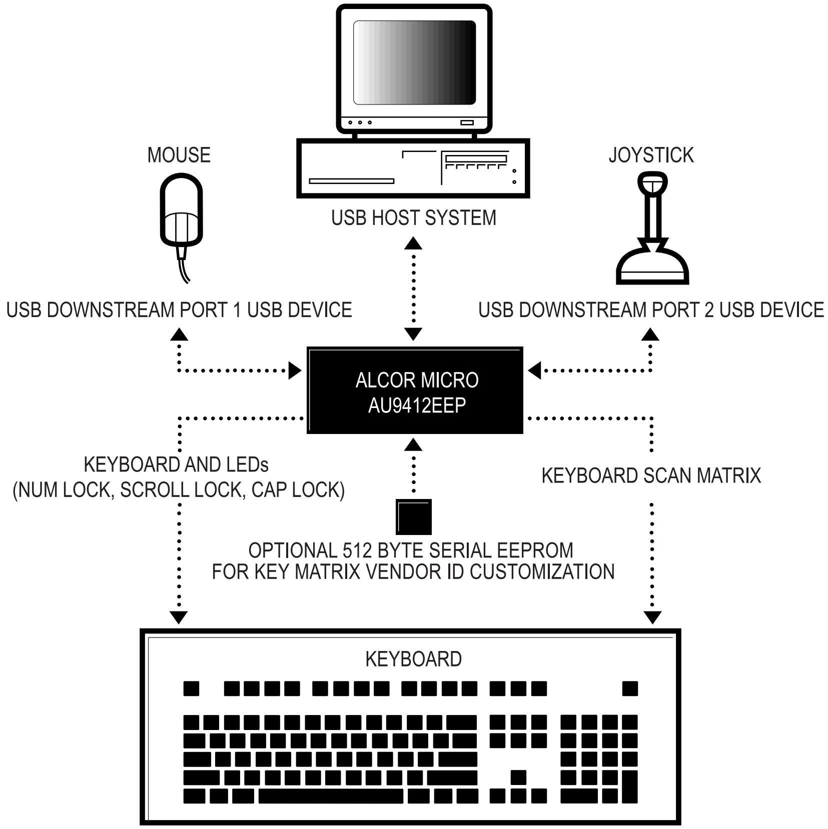
1.2. Features

- Fully compliant with the Universal Serial Bus Specification, version 1.0
- USB hub design is compliant with Universal Serial Bus Hub Specification, revision 1.1
- USB keyboard design is compliant with USB Device Class Definition for Human Interface Devices (HID), Firmware Specification, version 1.0
- Single chip integrated USB keyboard/hub controller with embedded proprietary processor
- Integrated USB hub supports two bus-powered downstream ports
- Patent-pending, table-driven SCANTABLE™ technology for easy customization to different keyboard matrix
- USB vendor ID, product ID, and keyboard scan code table can be customized via external EEPROM
- Built-in, cost saving, default scan code table and vendor ID, if customization is not necessary
- Built-in 3.3v voltage regulator allows single +5V operating voltage drawing directly from USB bus. This results in reduced overall system cost.
- Optional gang-powered control pin for downstream port.
- Runs at 12Mhz frequency
- Available in 48-pin DIP

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2.0 Application Block Diagram

The AU9412EEP is a single chip which integrates USB keyboard and hub functionality. The upstream port is connected to the USB system. The downstream ports can be used for a mouse and joystick.



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3.0 Pin Assignment

The AU9412EEP is a 48-pin dual inline package (DIP). The following figure shows the signal names for each of the pins on the chip. The table on the following page describes each of the pin signals.

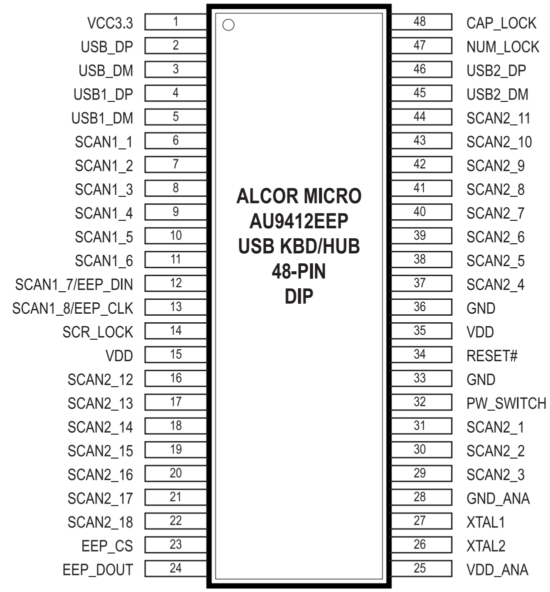


Table 3-1. Pin Descriptions

Pin #	Pin Name	I/O	Description
1	VCC3.3	O	3.3V output for upstream D+ pull-up; 4 mA
2	USB_DP	I/O	USB D+ for upstream port. Need external 1.5KΩ pull-up to 3.3V
3	USB_DM	I/O	USB D- for upstream port
4	USB1_DP	I/O	USB D+ for downstream port 1. Add 15KΩ pull-down to ground

Table 3-1 (continued). Pin Descriptions

Pin #	Pin Name	I/O	Description
5	USB1_DM	I/O	USB D- for downstream port 1. Add 15KΩ pull-down to ground
6	SCAN1_1	I	Matrix scan line; internal 3.3k pull-up
7	SCAN1_2	I	Matrix scan line; internal 3.3k pull-up
8	SCAN1_3	I	Matrix scan line; internal 3.3k pull-up
9	SCAN1_4	I	Matrix scan line; internal 3.3k pull-up
10	SCAN1_5	I	Matrix scan line; internal 3.3k pull-up
11	SCAN1_6	I	Matrix scan line; internal 3.3k pull-up
12	SCAN1_7/ EEP_DIN	I/O	Input: Matrix scan line; internal 3.3k pull-up. Output: EEPROM data in; connect to EEPROM DIN pin; 2 mA.
13	SCAN1_8/ EEP_CLK	I/O	Input: Matrix scan line; internal 3.3k pull-up. Output: Clock for EEPROM; 2 mA.
14	SCR_LOCK	O	Scroll Lock LED. Active low; 8 mA
15	VDD	PWR	+5v power supply
16	SCAN2_12	I/O	Matrix scan line; 16 mA, internal 33k pull-down
17	SCAN2_13	I/O	Matrix scan line; 16 mA, internal 33k pull-down
18	SCAN2_14	I/O	Matrix scan line; 16 mA, internal 33k pull-down

Table 3-1 (continued). Pin Descriptions

Pin #	Pin Name	I/O	Description
19	SCAN2_15	I/O	Matrix scan line; 16 mA, internal 33k pull-down
20	SCAN2_16	I/O	Matrix scan line; 16 mA, internal 33k pull-down
21	SCAN2_17	I/O	Matrix scan line; 16 mA, internal 33k pull-down
22	SCAN2_18	I/O	Matrix scan line; 16 mA, internal 33k pull-down
23	EEP_CS	O	Chip select, external EEPROM; 2 mA
24	EEP_DOUT	I	EEPROM data out; connect to EEPROM DOUT pin; 2 mA
25	VDD_ANA	PWR	Analog power; connect to +5V
26	XTAL2	O	Crystal oscillator; XTAL-out
27	XTAL1	I	Crystal oscillator; XTAL-in
28	GND_ANA	PWR	Analog Ground
29	SCAN2_3	I/O	Matrix scan line; 16mA, internal 33k pull-down
30	SCAN2_2	I/O	Matrix scan line; 16mA, internal 33k pull-down
31	SCAN2_1	I/O	Matrix scan line; 16mA, internal 33k pull-down
32	PW_SWITCH	O	Power switch control. Active low.
33	GND	PWR	Ground; VSS pad

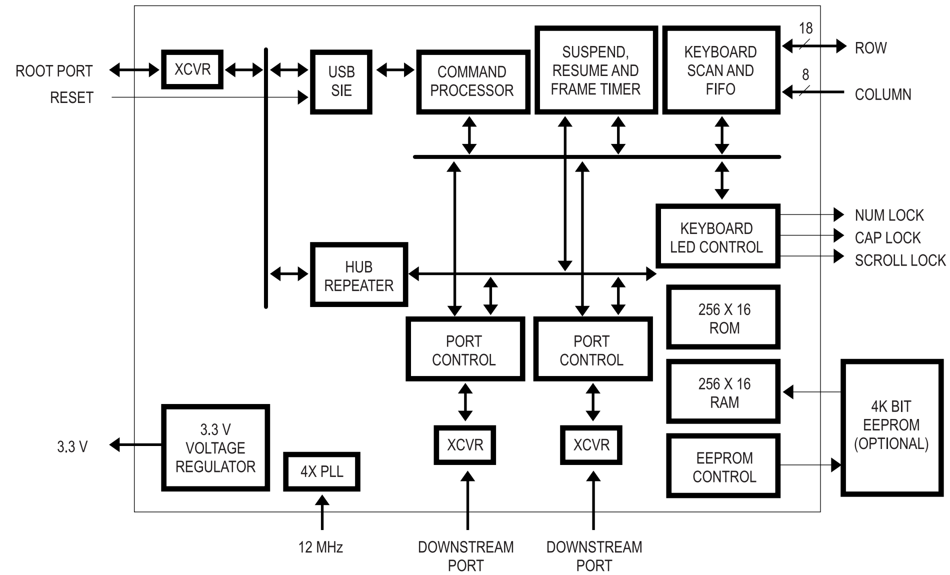
Table 3-1 (continued). Pin Descriptions

Pin #	Pin Name	I/O	Description
34	RESET#	I	Reset. Active low; Schmitt trigger input
35	VDD	PWR	+5v power; VDD pad
36	GND	PWR	Ground; VSS pad
37	SCAN2_4	I/O	Matrix scan line; 16mA, internal 33k pull-down
38	SCAN2_5	I/O	Matrix scan line; 16mA, internal 33k pull-down
39	SCAN2_6	I/O	Matrix scan line; 16mA, internal 33k pull-down
40	SCAN2_7	I/O	Matrix scan line; 16mA, internal 33k pull-down
41	SCAN2_8	I/O	Matrix scan line; 16mA, internal 33k pull-down
42	SCAN2_9	I/O	Matrix scan line; 16mA, internal 33k pull-down
43	SCAN2_10	I/O	Matrix scan line; 16mA, internal 33k pull-down
44	SCAN2_11	I/O	Matrix scan line; 16mA, internal 33k pull-down
45	USB2_DM	I/O	USB D- for downstream port 2. Add 15KΩ pull-down to ground
46	USB2_DP	I/O	USB D+ for downstream port 2. Add 15KΩ pull-down to ground
47	NUM_LOCK	O	Keyboard NUM_LOCK LED. Active low; 8 mA
48	CAP_LOCK	O	Keyboard CAP_LOCK LED. Active low; 8 mA

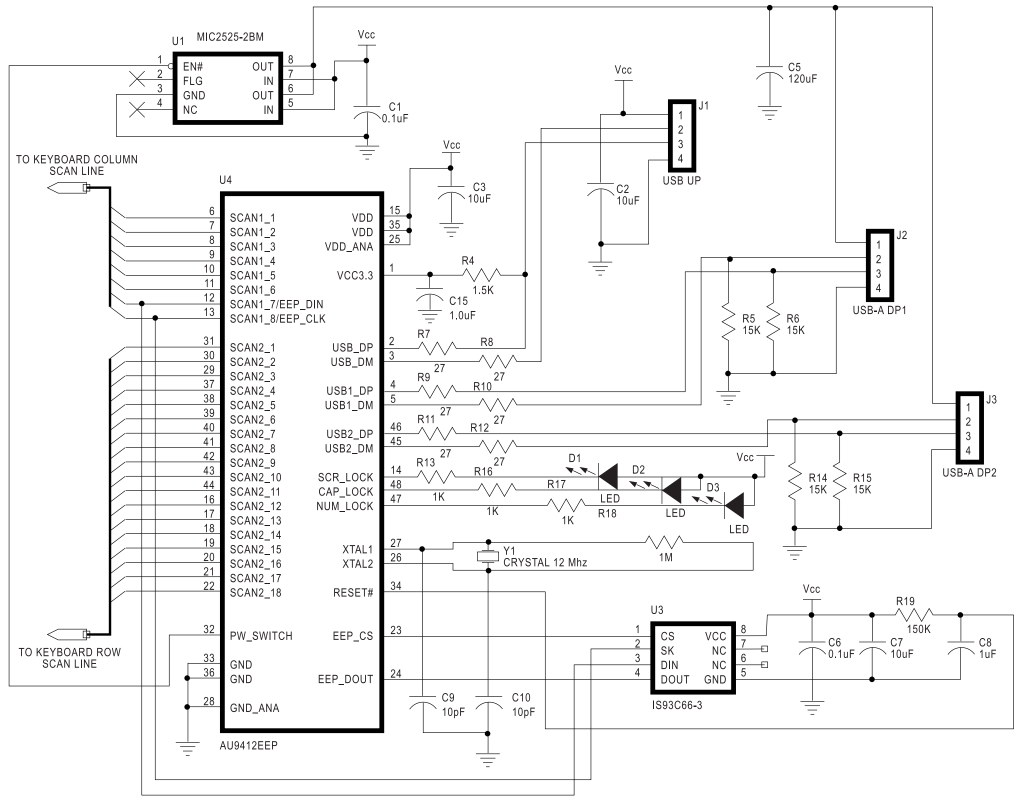
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4.0 System Architecture and Reference Design

4.1. AU9412EEP Block Diagram



4.2. Sample Schematics



4.3. Sample Key Matrix Layout Table

This table is the default key matrix. The AU9412EEP can support this matrix without an external EEPROM.

Table 4-1. AU9412 Built-in Key Matrix

	H1	H2	H3	H4	H5	H6	H7	H8
V1	Pause				Ctrl_R		Ctrl_L	F5
V2	Q	Tab	A	ESC	Z		~	1
V3	W	Caps	S		X		F1	2
V4	E	F3	D	F4	C		F2	3
V5	R	T	F	G	V	B	5	4
V6	U	Y	J	H	M	N	6	7
V7	I	}	K	F6	<		+	8
V8	O	F7	L		>	APP	F8	9
V9	P	{	:	“		/	-	0
V10	Scr_Lock			Alt_L		Alt_R		Prt_Sc
V11		BackSpace	|	F11	Enter	F12	F9	F10
V12	Kpd_Home	Kpd_4	Kpd_1	Space	Num Lock	Arrow_Dn	Del	
V13	Kpd_8	Kpd_5	Kpd_2	Kpd_0	Kpd_/	Arrow_Rt	Ins	
V14	Kpd_9	Kpd_6	Kpd_3	Kpd_.	Kpd_*	Kpd_-	PgUp	PgDn
V15	Kpd_+		Kpd_Enter	Arrow_Up		Arrow_Lt	End	End
V16		Shift_L	Shift_R					
V17		Win_L						
V18			Win_R					

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5.0 Electrical Characteristics

5.1. Maximum Ratings

Absolute Maximum Ratings

	VALUES	
PARAMETER	**MIN**	**MAX**
Ambient Operating Temperatures	0˚C	70˚C
Storage Temperature	-40˚C	185˚C
Supply Voltage (Vdd)	-0.3V	7.0V

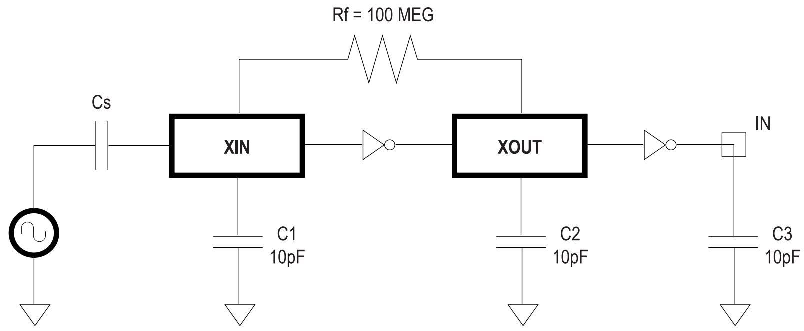
5.2. Recommended Operating Conditions

The following table gives the recommended operating conditions for integrated circuits developed with the pad libraries:

Symbol	Param.	Min	Max	V_{DD}	Note
V_{IL}	Low level input voltage	-0.5V	0.8V	4.5V to 5.5V	Guaranteed Input Low Voltage
V_{IH}	High level input voltage	2.0V	V_{DD}+0.5V	4.5V to 5.5V	Guaranteed Input High Voltage
V_{OL}	Low level output voltage		0.4V	4.5V	I_{OL}, 2 to 24 mA(TTL), depending on Cell
V_{OH}	High level output voltage	2.4V		4.5V	I_{OH}, 2 to 24mA(TTL) depending on Cell
I_{CC}	Supply current	20 mA	25 mA	4.5V to 5.5V	

5.3. Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.4. USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.5	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	˚C

ABSOLUTE MAXIMUM RATINGS 1, 2

In accordance with the Absoute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
V_{IK}	DC input diode current	Vi<0		-50	mA
V_{I}	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
V_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_{O}	DC output voltage	Note 3	-0.5	Vcc +0.5	V
V_{O}	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
V_{O}	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{GND}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STG}	Storage temperature range		-60	+/-150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicted under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40˚C to +86˚C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V	5.2	4.3	50.4	V
VIH	HIGH level input	Vcc=3.0V to 3.6V		15	20	V
VIL	LOW level input	Vcc=3.0V to 3.6V	0.5	11		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA		0.3	0.7 0.4 0.2	V
IQ	Quiecient supply current	Vcc=3.6V VI=Vcc or GND Io=0		330	600	µA
Isup	Supply current in suspend	Vcc=3.6V VI=Vcc or GND Io=0			70	µA
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Imput leakage current	Vcc=3.6V VI=5.5V or GND, not for I/O Pins		+/- 0.1	+/- 0.5	µA
IOFF	3-state output OFF-state current	VI=VIN or VII, Vo=Vcc or GND			+/-1-	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25˚C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

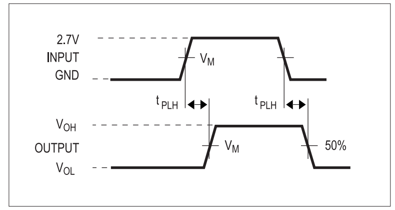
GND=0V, Is = IS=3.0 C=50pf, RL=500ohms

SYMBOL	PARAMETER	WAVFORM	LIMITS					UNIT
			-40˚C to +86˚C			-40˚C to +86˚C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
	Setup for SPEED	5	0					ns
Vcp	Crossover point[1]	3	1.3		2.0	1.3	2.0	V

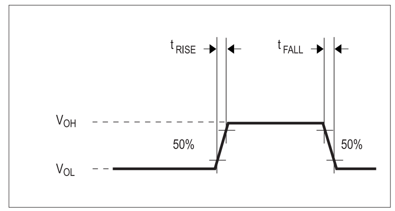
NOTE:

1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 5Cpf capacitance.

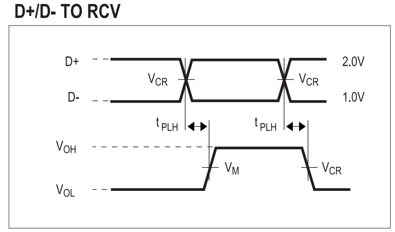
WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



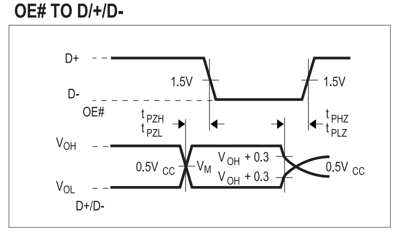
WAVEFORM 2.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



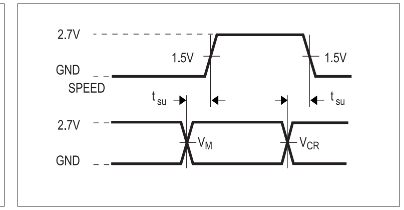
WAVEFORM 3.
D+/D- TO RCV



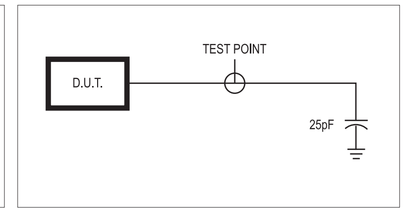
WAVEFORM 4.
OE# TO D/+/D-



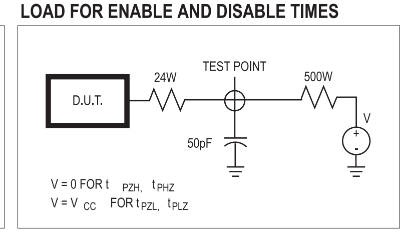
WAVEFORM 5.
SETUP FOR SPEED



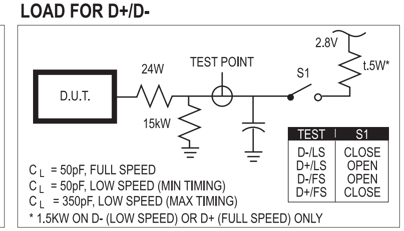
LOAD FOR VM/VP AND RCV



LOAD FOR ENABLE AND DISABLE TIMES



LOAD FOR D+/D-



5.5. ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test Circuit & Condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	2000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

5.6. Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

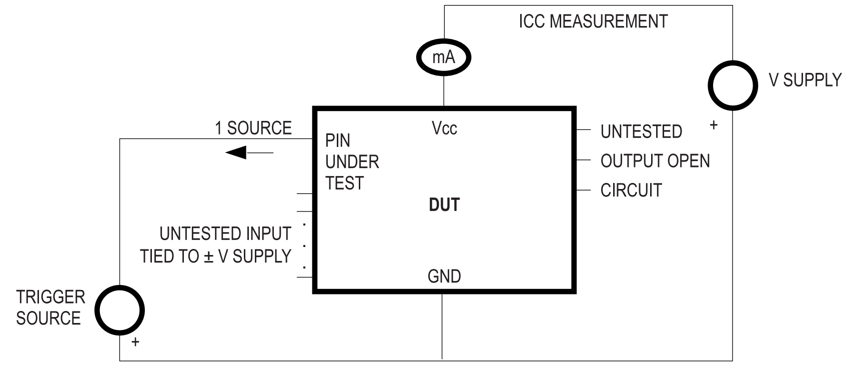
Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

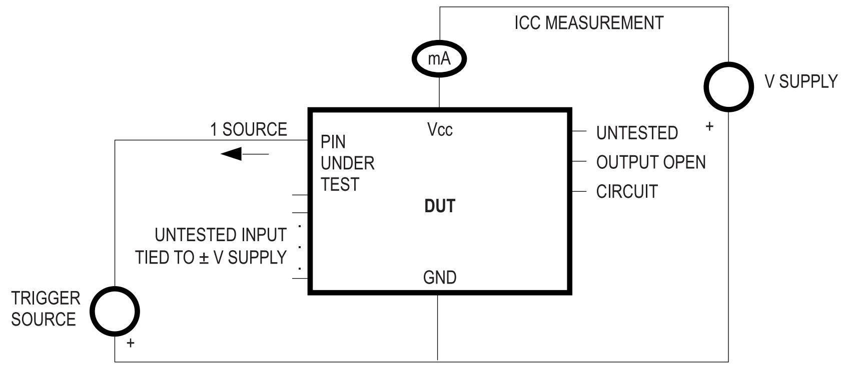
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:

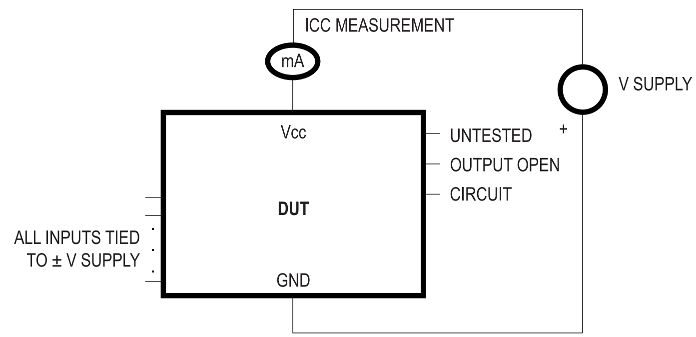
1. DUT: The device under test.
2. PUT: The pin under test.



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



Supply Overvoltage Test

Latch-Up Data

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

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6.0 Mechanical Information

Following diagram shows the dimensions of Alcor AU9412EEP 48-DIP package. Measurements are in millimeters; measurements in parenthesis are in inches.

